A Tunable Low-Power Semi-Digital Interface Circuit for Capacitive Sensors with Calibration Procedure

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Abstract

A new technique and circuit topology is proposed to read the output of a capacitive sensor for lab-on-chip (LOC) applications. Through capacitance-to-time conversion, together with several digital blocks, a first-order sigma-delta interface is developed. By encoding the change in capacitance as the difference in time between the rising edges of two digital signals, a compact, low-power realization is achieved. Moreover, the design is tunable along three axes: power, resolution and range. A digital calibration procedure is provided that exploits these three degrees of tuning and enables the design to be optimized for a desired capacitance range. A circuit has been fabricated in a 1-V 90-nm ST CMOS process requiring 120 μm x 20 μm footprint. Tests were conducted with on-chip capacitance ranging from 12.5 fF to 8 pF and the circuit was shown to be capable of measuring this full range of capacitance in a piecewise manner with a power consumption of 34 μW.

Keywords

Capacitive Sensors; Interface; Digital; Low-power; Calibration

Introduction

Capacitive sensing that is used extensively in a wide range of micro-electromechanical sensors (MEMS) offers low-power operation, high sensitivity, low temperature variation, simple structure and the option of applying electrostatic actuation for closed-loop control [Baxter 1997, Kulah 2006].

Due to the high impedance nature of a capacitor at low frequencies, capacitive sensing is susceptible to parasitic components and noise at the interface between the readout circuit and the capacitor [Yazdi 2004]. The design of the readout circuit cannot be initiated until the specification of the sensor is finalized and the measurement range is determined. One approach is to make use of a bank of on-chip capacitors at the expense of silicon area to compensate digitally for processing errors. Another approach identified in [Preethichandra 2001] is the on-chip reference capacitor implemented through a resistor-tunable gyrator circuit; however, on-chip resistors like capacitors provide no additional tuning ability.

Practical sensors generally do not include the readout electronics on the same die; instead, they are assembled together in multi-chip packages. As a result, the interconnection parasitic capacitance may evoke sensor repeatability errors and create offsets. In [Kulah 2006, O'Dowd 2005, and Lee 2007] some advanced switched-capacitor (SC) circuits have been reported, whereby the resolution of the readout circuit has been developed as low as 10 aF with parasitic compensation. Applications of an AC bridge with voltage amplification [Constandinou 2008] and trans-impedance amplification [Geen 2002] are two other techniques previously reported. These circuits are reported of measuring a capacitance change of less than 1 fF. To achieve such low resolution, additional circuit elements and techniques are included to control or cancel charge injection effects and component mismatching effects, requiring large amounts of silicon area and power [Takahata 2004]. The charge-based capacitance-measurement approach (CBCM) [Sutory 2007] eliminates the need for a reference capacitor but requires an accurate current measurement.

When the sensor is integrated directly alongside the readout electronics, the silicon-substrates typically suffer from poor uniformity, forcing transistor parameter-variations to rise [Dimitropoulos 2006, Ylimaula 2003]. Adopting a digital signaling approach, the readout electronics can be constructed from digital gates, such as inverters, flip-flops, etc., so that process variations can be more easily calibrated out. In [Xiaojing 2001], although the authors have claimed a digital readout technique, the front-end of the design is largely op-amp based. In [Wu 2004], a digital-compatible technique is presented; however, the method is applicable to

differential capacitive sensors only and requires power-hungry high-frequency clocks for fine resolution.

An increasing number of medical, entertainment and sports applications has made use of sensor systems in and around the body. These sensors should work as distributed small units that can collect data over a long period and consume ultra-low power [Bracke 2007]. Many of the sensor interfaces previously reported are fixed designs, tailored towards one specific application. Enabling sensor interface circuits that are suited for a wider range of applications would help to reduce the cost of such circuits and speed their time-to-market. In some ways, a more generic topology for a sensor interface circuit is required and is the focus of this paper.

The paper is organized as follows: the general operation and principles of the proposed sensor interface circuit are described in section II. In section III, the tuning procedure for the calibration and setting of the circuit is presented. Section IV, provides the experimental results for the fabricated chip; and finally, section V summarizes the paper and the conclusions are drawn.

Delta-Sigma Interface for Capacitive Sensors

Capacitance-t-Time Conversion

The voltage drop across the pre-charged capacitor in Fig. 1(a) being discharged by a constant current, $I_{Discharge}$, is well defined using the equation

$$V_C(t) = V_{DD} - \frac{C}{I_{Discharge}} \times t \quad (1)$$

By changing the capacitor, the slope of the discharge procedure changes linearly. By adding an inverter in cascade to the capacitor, the delay between the digital rising edges at Φ_{IN} and Φ_{OUT} can be calculated using

$$\tau_{Delay} = \frac{C \times (V_{DD} - V_{Th,inv})}{I_{Discharge}} \quad (2)$$

where $V_{Th,inv}$ is the threshold voltage of the inverter. For ease of reference, the delay is related to the capacitance variable using a proportionality coefficient, G_{φ}, as

$$\tau_{Delay} = G_{\varphi} C \quad (3)$$

Clearly, the delay of the circuit shown in Fig. 1(a) is linear in terms of the capacitor value and the block may be called a Capacitance-Controlled Delay Unit (CCDU). In Fig. 1(b), a CMOS circuit schematic to implement a CCDU is presented. The AND gate is used to ensure that the input falling edge at Φ_{IN} is propagated to the output without being influenced by the control capacitor; also, transistor M_4 is included to discharge the control capacitor quickly and to bypass the delay of the block, where applicable. Fig. 2 shows the circuit symbol for the developed CCDU.

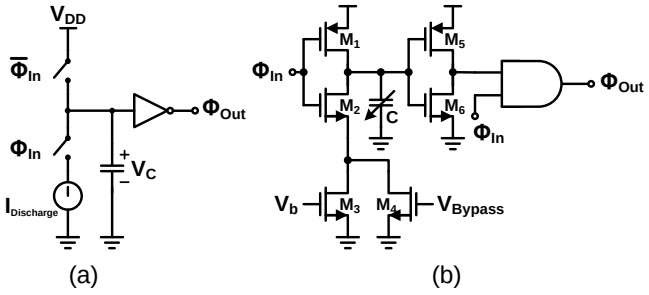


FIG. 1 (a) THE LINEAR DISCHARGE OF A CAPACITOR, (b) CIRCUIT DIAGRAM FOR A CAPACITANCE-CONTROLLED DELAY UNIT (CCDU)

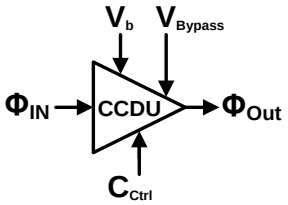


FIG. 2 THE CIRCUIT SYMBOL FOR A CCDU

Adopting the linear capacitance-to-time conversion, a time-mode output will be produced that is the time difference between the digital rising edges at the input and output of the proposed CCDU. Due to the digital nature of the signals, digital circuits can be used alongside the CCDU to estimate the input capacitance. Using this technique, in the rest of this paper the detailed design of a first-order time-mode sigma-delta interface to readout the output of a capacitive sensor will be covered.

Capacitance-to-Time Integration

Integrators are the most fundamental building blocks in any sigma-delta architecture. To proceed with the design of the sigma-delta interface, a capacitance-to-time integrator can be implemented by connecting the outputs of two CCDUs to their respective inputs through two inverters. This circuit is equivalent to two capacitance-controlled ring oscillators and is depicted in Fig. 3(a). Considering C_{IN} (the capacitance subject to measurement) equal to C_{REF}, the delay induced by these two blocks will be the same; so that, the oscillation periods for the oscillating signals at Φ_{SIG} and Φ_{REF} will be the same. Writing the arrival time of the *n-th* rising edge at the output of each CCDU in terms of the arrival time of the respective rising edge at the input of the same CCDU, we can write

$$t_{SIG}[n] = t_I[n-1] + G_\varphi C_{IN}[n-1] \quad (4)$$

and

$$t_{REF}[n] = t'_I[n-1] + G_\varphi C_{REF} \quad (5)$$

where, t_I (t'_I) and t_{SIG} (t_{REF}) represent the arrival time for the rising edges at the inputs and outputs of $CCDU_1$ ($CCDU_2$) respectively. Furthermore, the feedback path established by the inverter allows us to state

$$t_I[n-1] = t_{SIG}[n-1] + \tau_{CCDU} + 2\tau_{INV} \quad (6)$$

and

$$t'_I[n-1] = t_{REF}[n-1] + \tau_{CCDU} + 2\tau_{INV} \quad (7)$$

where, $\tau_{CCDU} + 2\tau_{inv}$ is the total propagation delay of a low-to-high transition at the CCDU output back to its inputs as a low-to-high transition. Combining Eqns. (4)-(7), we can write

$$t_{SIG}[n] = t_{SIG}[n-1] + G_\varphi C_{IN}[n-1] + \tau_{CCDU} + 2\tau_{INV} \quad (8)$$

and

$$t_{REF}[n] = t_{REF}[n-1] + G_\varphi C_{REF} + \tau_{CCDU} + 2\tau_{INV}\,. \quad (9)$$

Finally, by subtracting Eqn. (9) from Eqn. (8), we obtain

$$\begin{aligned} \Delta T_{OUT}[n] &= t_{SIG}[n] - t_{REF}[n] \\ &= \Delta T_{OUT}[n-1] + G_\varphi C_{IN}[n-1] \end{aligned} \quad (10)$$

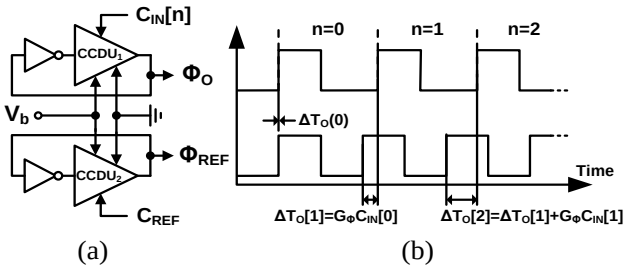


FIG. 3 (a) CAPACITANCE-TO-TIME INTEGRATOR. (b) TIMING DIAGRAM FOR THE INTEGRATOR

Here, $\Delta T_{OUT}[n]$ represents the time difference between the rising edges at the outputs of the two oscillators. A timing diagram demonstrating three samples of the integrator operation is presented in Fig. 3(b). The initial integrator output time-difference, i.e. $\Delta T_{OUT}[0]$, is assumed equal to zero. The next time-difference $\Delta T_{OUT}[1]$ is shown proportional to the input capacitance at time instance $n=0$. The proceeding output $\Delta T_{OUT}[2]$ is the sum of $\Delta T_{OUT}[1]$ and the input capacitance $C_{IN}[1]$ scaled by G_φ.

Sigma-Delta Interface

The developed capacitance-to-time integrator of Fig. 3(a) can be extended to a first-order sigma-delta modulator based on the error-feedback structure presented in Fig. 4 [Ali-Bakhshian 2009]. The output comparator by checking the sign of the output phase difference, i.e. $\Delta T_{OUT}[n]$, represents a single-bit quantizer. A D-type Flip/Flop (DFF) can be used as the output comparator. If the rising edge at the clock input leads the rising edge at the D input (for a negative phase difference), the output will be set to "0"; otherwise, for a positive phase difference it will be set to "1". To implement the DAC feedback included in Fig. 4, the output bit should be applied directly to the bypass input of one of the CCDUs in the ring oscillators. This will cause the delay of the corresponding CCDU to be excluded from the loop delay when the DFF output D_O is "1", as well force the instantaneous period of the oscillation at the output of the corresponding oscillator to decrease. Otherwise, the propagation delay of this CCDU will be accumulated into the overall loop delay.

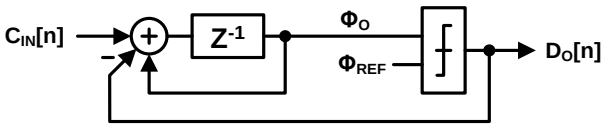


FIG. 4 BLOCK DIAGRAM FOR A FIRST-ORDER DELTA-SIGMA MODULATOR

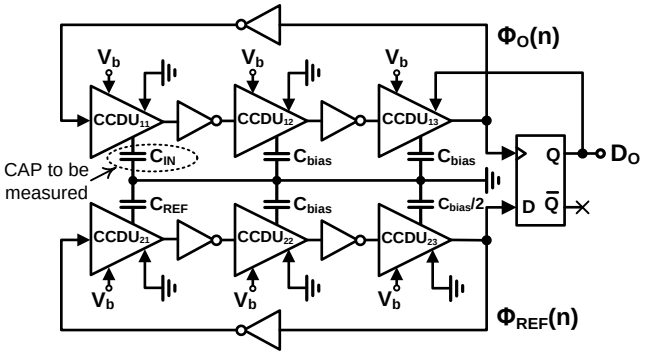


FIG. 5 THE CIRCUIT SCHEMATIC FOR THE PROPOSED FIRST-ORDER DELTA-SIGMA SENSOR INTERFACE CIRCUIT

The complete diagram of the proposed sigma-delta-based interface is presented in Fig. 5 and it consists of two ring-oscillators and one DFF. For ease of reference, the top and the bottom oscillators will be referred to as the signal and the reference oscillators respectively. All CCDUs are biased at the fixed bias voltage of V_b. $CCDU_{11}$ and $CCDU_{21}$ operate as the input stage to convert the capacitance difference between C_{IN} and C_{REF} to a phase difference between the two oscillators. $CCDU_{13}$ and $CCDU_{23}$ with different control capacitors equal to C_{bias} and $C_{bias}/2$ are considered to implement the feedback. Finally, $CCDU_{12}$ and $CCDU_{22}$ with identical control capacitors equal to C_{bias} are included to set the duty cycle of the oscillating signal in each oscillator. Except for the bypass input to $CCDU_{13}$ that is connected to the output of the DFF, all other CCDU bypass inputs are connected to ground.

As the discharge current, $I_{Discharge}$, adopted in Eqn. (2) is

controlled by V_b, this equation can be rewritten in general terms as a function of the bias voltage, i.e.

$$\tau_{Delay} = C \times f(V_b). \quad (11)$$

Now returning to the circuit of Fig. 5, the period of each oscillator can be derived by considering the propagation delay around each loop. In the case of a falling edge at the output of the reference oscillator, the propagation delay around the loop to invert it back to a rising edge equals

$$T_{REF,Low} = 3\tau_{inv} + C_{REF} \times f_{21}(V_b) + \tau_{CCDU22} + \frac{C_{bias}}{2} \times f_{23}(V_b) \quad (12)$$

where, we make use of the delay-V_b functional notation of Eqn. (11) for each CCDU in the loop. Likewise, the rising edge at the output of the reference oscillator comes back as a falling edge after

$$T_{REF,High} = 3\tau_{inv} + \tau_{CCDU21} + C_{bias} \times f_{22}(V_b) + \tau_{CCDU23}. \quad (13)$$

Apparently, the total period of any single oscillation at the output of the reference oscillator is

$$T_{REF} = T_{REF,Low} + T_{REF,High}. \quad (14)$$

Similar equations can be extracted for the signal oscillator as

$$T_{SIG,Low} = 3\tau_{inv} + C_{IN} \times f_{11}(V_b) + \tau_{CCDU12} + (1 - D_O) \times C_{bias} \times f_{13}(V_b). \quad (15)$$

and

$$T_{SIG,High} = 3\tau_{inv} + \tau_{CCDU11} + C_{bias} \times f_{12}(V_b) + \tau_{CCDU13} \quad (16)$$

so that the total period for any single oscillation at the output of the signal oscillator is given by

$$T_{SIG} = T_{SIG,Low} + T_{SIG,High}. \quad (17)$$

Fig. 6 shows the timing signals for each oscillator output, Φ_{SIG} and Φ_{REF}. The reference oscillator provides the clock reference for the output comparator and its oscillation period is constant and independent of the input capacitance C_{IN} and DFF state, D_O. In contrast, the low-level width of the signal at Φ_{SIG} is a function of both C_{IN} and D_O; thus making the period of this oscillator a function of the capacitance subject to measurement. As the DFF quantizes the accumulated time difference between the instantaneous periods of the two oscillator outputs, we can write

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + T_{SIG}[n] - T_{REF} \quad (18)$$

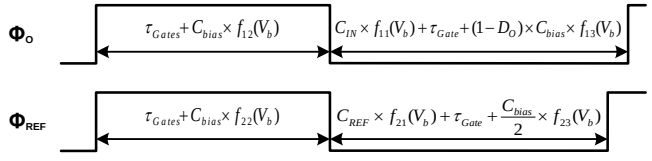


FIG. 6 THE DURATION OF A SINGLE PERIOD OF THE SIG AND REF OSCILLATORS

Substituting Eqns. (14) and (17), together with Eqns. (12), (13), (15) and (16) leads to a recursive expression for the instantaneous output time-difference $T_{OUT}[n]$. In an ideal situation, $CCDU_{11}$ identical to $CCDU_{21}$, $CCDU_{12}$ can be assumed identical to $CCDU_{22}$, and $CCDU_{13}$ identical to $CCDU_{23}$. By considering the $f(V)$ function representing each identical pair as $f_1(V_b)$, $f_2(V_b)$, and $f_3(V_b)$ respectively, the resulting expression becomes

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + (C_{IN}[n-1] - C_{REF}) \times f_1(V_b) + C_{bias} \times f_3(V_b) \times \left\{ \frac{1}{2} - D_O[n-1] \right\} \quad (19)$$

Assuming $D_O[n]$ is a digital signal toggling between "0" and "1", the error signal $\Delta T_\varepsilon(n)$ induced by the DFF comparison may be expressed as the difference between the instantaneous output time difference and the size of the delay injected back into the loop, i.e.,

$$\Delta T_\varepsilon[n] = \Delta T_{OUT}[n] - C_{bias} \times f_3(V_b) \times \left\{ D_O[n] - \frac{1}{2} \right\} \quad (20)$$

Substituting Eqn. (20) into (19) reveals the first-order $\Delta\Sigma$ modulator difference equation as

$$D_O[n] = \frac{f_1(V_b)}{C_{bias} \times f_3(V_b)} \{ C_{IN}[n-1] - C_{REF} \} - \frac{1}{C_{bias} \times f_3(V_b)} \{ \Delta T_\varepsilon[n] - \Delta T_\varepsilon[n-1] \} + \frac{1}{2}. \quad (21)$$

Fig. 7 presents an example illustrating the timing of four periods of the modulator's operation with input condition, $C_{IN} = C_{REF}$. The period of oscillation for Φ_{REF} is fixed; also, the high-level width of the oscillating signal at Φ_{SIG} is fixed at $T_{SIG,High}$. Here, it can be seen that how the low-level width of this signal toggles with constant input capacitance and DFF output.

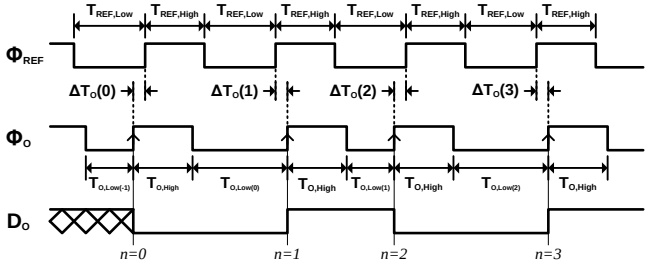


FIG. 7 TIMING DIAGRAM OF A SHORT SEQUENCE OF THE DELTA-SIGMA OPERATION

Linear Range of Operation

C_{REF} is the reference value for the input capacitance C_{IN} and the system is designed to measure any capacitance variation compared to C_{REF}. By substituting $C_{IN}[n] = C_{REF} + \Delta C[n]$ into Eqn. (19), one can write an expression for the modulator output as:

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + \Delta C \times f_1(V_b) + C_{bias} \times f_3(V_b) \times \left\{ \frac{1}{2} - D_O[n-1] \right\} \quad (22)$$

For stable sigma-delta operation, the input amplitude of the modulator should be smaller than that of the feedback signal; so that the latter two terms associated with Eqn. (22) must undergo a full sign change. When the DFF output is in logic "0" state, we should have

$$\Delta C \times f_1(V_b) + C_{bias} \times \frac{f_3(V_b)}{2} > 0 \tag{23}$$

Similarly, when D_O="1", we should have

$$\Delta C \times f_1(V_b) - C_{bias} \times \frac{f_3(V_b)}{2} < 0 \tag{24}$$

which leads to the following condition on the input capacitance for linear operation:

$$-\frac{C_{bias}}{2} \times \frac{f_3(V_b)}{f_1(V_b)} < \Delta C < \frac{C_{bias}}{2} \times \frac{f_3(V_b)}{f_1(V_b)}. \tag{25}$$

As $T_{SIG,Low}$ is a function of the input capacitance and state of the DFF, it can take on different values. If this time is longer than a period of the reference oscillator, as depicted in Fig. 8, it is possible to lose one full cycle of the reference oscillator, e.g., create a cycle slip. To avoid such a condition, the timing for both oscillator outputs should satisfy the following relation,

$$T_{High} + T_{SIG,Low}\big|_{D_O=0} \le 2T_{High} + T_{REF,Low} \tag{26}$$

where we assume T_{High}= $T_{REF,High}$= $T_{SIG,High}$. Substituting corresponding expressions for each variable in Eqn. (26) results in a further simplified expression as

$$T_{High} \ge \Delta C \times f_1(V_b) + \frac{C_{bias}}{2} \times f_3(V_b). \tag{27}$$

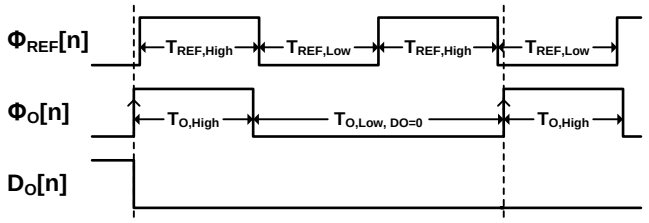


FIG. 8 THE FEEDBACK PUSHING THE CIRCUIT OUT OF LINEAR OPERATION

The inequality shown in Eqn. (27) should be satisfied even for the largest value of the input capacitance specified by (25); ignoring the minor values for gate delays, and Eqn. (27) can be reduced to

$$f_2(V_b) \ge f_3(V_b) \tag{28}$$

This expression indicates that for the same control capacitor, C_{bias}, the delay induced by $CCDU_{12}$ and $CCDU_{22}$ should be equal or greater than the delay induced by $CCDU_{13}$ and $CCDU_{23}$.

Satisfying inequality Eqn. (25) and Eqn. (28), the sensor interface operates in its linear mode and the error term ΔT_ε in Eqn. (21) will be removed through noise-shaping and averaging. As a result, the average value of the digital output will be equal to

$$\langle D_O \rangle = \frac{f_1(V_b)}{C_{bias} \times f_3(V_b)} \Delta C + \frac{1}{2} \tag{29}$$

where < > denotes the average value. In Fig. 9, the transfer characteristic of the sensor interface circuit is shown. Here the limits of the input differential capacitance are provided in terms of the C_{bias} and the bias voltages V_b. Also shown is the dependency of the slope (or gain) of the linear region in terms of these same two quantities. Outside of the linear region, the average value of digital output will be uncorrelated to the input capacitance and its value is invalid.

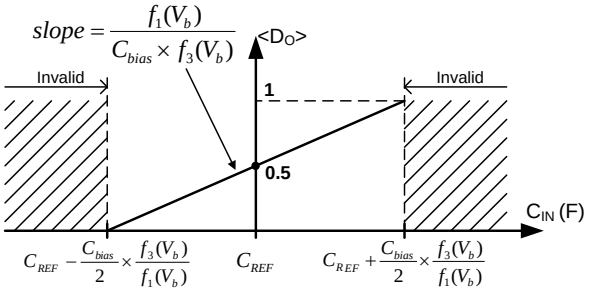


FIG. 9 TRANSFER CHARACTERISTIC OF THE SENSOR INTERFACE CIRCUIT

Noise Behavior

To characterize the effect of noise on the overall performance of the sensor interface circuit, two independent noise sources $v_{n,b}$ and $v_{n,d}$ are considered accompanied with the voltages V_b and V_{DD} in Fig. 1(b). Since transistor M_3, on the same figure, operates in the saturation region, while the formula governing the discharge current can be written as

$$I_D = \beta(V_b + v_{n,b} - V_{Th3})^2 \tag{30}$$

Expanding Eqn. (30) as a power series,

$$I_D = \beta(V_b - V_{Th3})^2 + 2\beta(V_b - V_{Th3})V_{nb} + \beta V_{nb}{}^2 \tag{31}$$

with condition $v_{n,b} << V_b - V_{Th3}$, we can ignore the last term and write the discharge current as

$$I_D = I_{Discharge} + K_n v_{n,b}. \tag{32}$$

Here, $I_{Discharge}$ is the original discharge current without taking noise into account and $K_n = 2\beta(V_b - V_{Th3})$. Substituting the above equation in Eqn. (2) and considering the noise source $v_{n,d}$ associated with V_{DD}, the delay formula influenced by noise will be

$$\tau_{Delay,noise} = \frac{C \times (V_{DD} + v_{n,d} - V_{Th})}{I_{Discharge} + K_n v_{n,b}} \tag{33}$$

Provided , Eqn. (33) can be expanded using a binomial expansion, leading to

$$\tau_{Delay,noise} = \frac{C \times (V_{DD} - V_{Th} + v_{n,d})}{I_{Discharge}} \left(1 - \frac{K_n v_{n,b}}{I_{Discharge}} + \frac{K_n^2 v_{n,b}^2}{I_{Discharge}^2} ...\right) \tag{34}$$

Considering Eqn. (2) and ignoring the second and higher order components in (34), the formula for delay of a CCDU block can be written as the sum of a noise-free term and a noise component, i.e.

$$\tau_{Delay,noise} = \tau_{Delay} + \tau_{Noise} \quad (35)$$

where τ_{Noise} is given by

$$\tau_{Noise} = \frac{C}{I_{Discharge}} v_{n,d} - \frac{\tau_{Delay} K_n}{I_{Discharge}} v_{n,b} + \frac{K_n C}{I_{Discharge}^2} v_{n,b} v_{n,d} \quad (36)$$

Assuming that $v_{n,b}$ and $v_{n,d}$ are two noise sources uncorrelated with zero mean value, the expected value of the jitter will be equal to zero and the mean square value of the jitter will be

$$\sigma_\tau^2 = \frac{C^2}{I_{Discharge}^2} \sigma_{v_{n,d}}^2 + \frac{\tau_{Delay}^2 K_n^2}{I_{Discharge}^2} \sigma_{v_{n,b}}^2 \quad (37)$$

The delay around each loop is the summation of the delays of the CCDUs in that loop. So, each oscillating signal undergoes the same type of jitter as a single CCDU block, albeit with some scaling coefficient between 1 and 3. Hence, Eqn. (37) provides the key noise behavior of each oscillator.

Impact of Temperature

Due to temperature gradient over the wafer, the threshold voltage of the transistors and the mobility of the charge carriers are subject to change. As shown in the section for the experimental results, the footprint of the implemented design is very small. This guarantees that by adopting some basic matching techniques such as common-centroid or interdigitized structures, corresponding CCDUs in both oscillators undergo the same temperature variation; so that the temperature-dependant mismatches between the oscillators will be negligible. Also, as temperature changes $f_1(V_b)$ in Eqn. (29) change in the same direction as $f_3(V_b)$; consequently, the temperature sensitivity of the output, i.e. $\langle D_O \rangle$ that is equal to the ratio of these two values can be designed to be quite small.

Impact of Transistor Mismatches

The architecture of the proposed circuit is differential and the reference and signal oscillators are supposed to be identical but have different control capacitors. However, mismatches are unavoidable in any CMOS process and it is impossible to have the two ring-oscillators completely matched. As shown in Fig. 5, each component contributes to the overall performance of the modulator by the propagation delay of the signal passing through that component. Mismatches between the threshold voltages, discharge currents, dimensions, and etc of the corresponding elements in two oscillators will show up as the difference between their loop delays. By considering a different $f(V_b)$ for each individual CCDU to model the mismatch effect and by reviewing the steps taken to extract Eqn. (29), this equation changes as

$$D_O[n] = \frac{K_{MMatch} \times f_1(V_b)}{C_{bias} \times f_3(V_b)} \left(C_{IN}[n-1] - C'_{REF} \right) + \frac{1}{2}. \quad (38)$$

Apparently, mismatches change the slope of the transfer characteristic by a factor of K_{MMatch}; also, the effective value for the C_{REF} changes to C'_{REF}. These changes, however, are independent of the input capacitor and they do not result in any non-linearity. As explained in the next section, the effect of mismatches can be easily calibrated through a tuning procedure on start-up.

Tuning and Controlling the Sensor Interface Circuit

Changing CREF and the range/sensitivity of the circuit

As previously explained, each pair of CCDUs adopted in the sensor interface circuit was presented by a different function as $f_1(V_b)$, $f_2(V_b)$, or $f_3(V_b)$. By controlling each individual CCDU, more control over the range of operation and sensitivity of the circuit will be possible. For the rest of this paper, $CCDU_{11}$ and $CCDU_{21}$ will be represented by different functions $f_{11}(V_b)$ and $f_{21}(V_b)$, respectively, and Eqns. (25) and (29) will change accordingly as

$$-\frac{C_{bias}}{2} \times \frac{f_3(V_b)}{f_{11}(V_b)} < \Delta C < \frac{C_{bias}}{2} \times \frac{f_3(V_b)}{f_{11}(V_b)}. \quad (39)$$

and

$$\langle D_O \rangle = \frac{f_{11}(V_b)}{C_{bias} \times f_3(V_b)} (C_{IN} - C_{REF}) + \frac{1}{2} \quad (40)$$

As explained in the previous sections, each control capacitor contributes to the circuit by influencing the partial delays around each loop, as formulated by Eqn. (11). By changing C_{REF} in the modulator shown in Fig. 5 to $n \times C_{REF}$, the delay induced by $CCDU_{21}$ will be equal to

$$\tau_{Delay21} = n \times C_{REF} \times f_{21}(V_b), \quad (41)$$

which can be rewritten as

$$\tau_{Delay21} = C_{REF} \times f_{21}(V'_b), \quad (42)$$

Eqns. (41) and (42) indicate that there are two ways in which the same delay can be achieved. One is to use a capacitance of $n \times C_{REF}$ and the other way is to use a different bias voltage of V'_b. By increasing V_b, the

magnitude of $f(V_b)$ decreases; consequently, for a fixed value of C_{REF} the delay induced by this capacitor decreases. So, the bias voltage applied to CCDU21 can be used to change the effect of the reference capacitance of the sensor interface circuit while the range of operation and the sensitivity of the sensor interface circuit do not change. To proceed with this idea, the new concept of equivalent capacitance reference level, $C_{REF,EQV}$, can be defined as

$$C_{REF,EQV} = C_{REF} \times n_{21}(V'_b), \quad (43)$$

and $n_{21}(V'_b)$ represents the scaling factor controlled by the bias voltage connected to CCDU21.

The same process might be implemented to modify the sensitivity of the sensor interface circuit. With respect to Eqn. (40), for the same output range, scaling the numerator term $f_{11}(V_b)$ by some factor, say α, the input differential capacitance C_{IN}-$C_{REF,EQV}$ can be scaled by the factor $1/\alpha$. This situation is depicted in Fig. 10 for two different bias conditions V_{b1} and V_{b2} when $V_{b1} < V_{b2}$. Here we make use of the functional representation

$$\lambda(V_b) = \frac{C_{bias}}{2} \frac{f_3(V_b)}{f_{11}(V_{b2})} \quad (44)$$

$$K_n v_{n,b} < I_{Discharge}$$

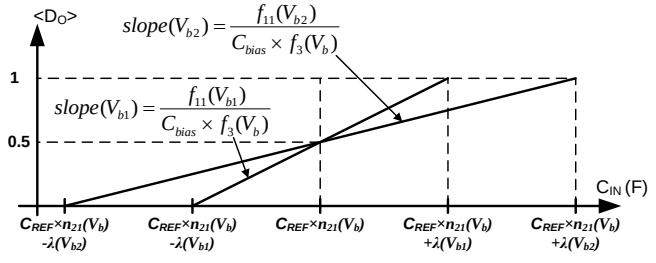


FIG. 10 TRANSFER CHARACTERISTIC OF THE SENSOR INTERFACE CIRCUIT FOR TWO DIFFERENT BIAS CONDITIONS ON CCDU11

In effect, changing the bias voltage of CCDU21 changes the equivalent reference capacitance and changing the bias of CCDU11 changes the sensitivity of the circuit. Collectively, these two control variables enable the circuit to operate over a wide range of input capacitance conditions.

The reader may be worried about the number of design specs and control variables to be set; however, all this information is included to demonstrate the flexibility of the proposed design. In an application–oriented design and based on the degrees of freedom required, the transfer characteristic of the interface circuit can be simplified by ignoring some of the above tunablity features.

The Detection of Non-linear Operation

If the sensor interface behaves linearly, for each cycle of the signal oscillator there should be a corresponding cycle from the reference oscillator. If one of the rising edges is missing, it is good evidence that the input capacitance is out of linear range, as explained shortly. By observing the output of each oscillator, together with the state of the D-type F/F, a digital code can be devised that keeps track of the sequence of events occurring within the circuit. One component of the digital code consists of the order in which the rising edges appear at the output of each oscillator. For example, if the rising edge for the reference oscillator appears after the one for the signal oscillator and we denote the reference rising edge with symbol *"↑"* and the oscillator rising edge with symbol *"A"*, then one part of the output code would be written as *"A↑"*. If this sequence continues then the output code would appear as *"A↑A↑A↑…"*. The other component of this code consists of the state of the output D-type F/F at the rising edge of the signal oscillator. We combine these two code components by substituting symbol *"A"* by the corresponding state of the F/F. For instance, if the state of the F/F follows the sequence *"110"*, then the combined code would be *"1↑1↑0↑…"*.

When C_{IN} is less than the minimum value allowed, the period of the signal oscillator will be shorter than the period of the reference oscillator and even the feedback signal cannot change this condition. Similarly, if C_{IN} is greater than its maximum allowed value, the signal oscillator period will be longer than the period of the reference oscillator and the feedback signal cannot correct this situation either. These two situations result in a set of error codes that indicate nonlinear operation.

In Fig. 11(a) three situations are shown where the signal oscillator period is less than the reference oscillator period. Considering the first situation involving Φ_{REF} and Φ_{O1}, the maximum period of Φ_{O1} is slightly shorter than the period of Φ_{REF}; after a few cycles, two rising edges for Φ_{O1} happens within one cycle of Φ_{REF}. This situation results in the code sequence of *"0↑1"* representing the missing rising edge for Φ_{REF}. The correct sequence should have been *"0↑↑1"*. Another situation depicted by Φ_{O2} and Φ_{O3} captures the situation where the period of signal oscillator is much shorter and two successive rising edges of the signal oscillator may sample one identical digital level of Φ_{REF}. As a result, the sequence of *"11"* or *"00"* will be produced within the output. The appearance of each one of these three error codes

confirms that the input C_{IN} is less than the allowed minimum value. Similarly, Fig. 11(b) shows four situations when C_{IN} exceeds its maximum allowable value. Considering the first situation involving reference signal Φ_{REF} and signal oscillator Φ_{O1}, even after applying the feedback D_O="1", the period of signal oscillator is slightly greater than the period for reference oscillator. After a few cycles, one complete cycle of the reference oscillator will be missed and an error sequence of "1↓0" appears where the correct sequence is "10". Other situations depicted in Fig. 11(b) corresponding to C_{IN} being much greater than the upper bond and resulting in higher number of missed cycles are captured by signals Φ_{O2}, Φ_{O3}, and Φ_{O4}. In much the same way as described for the previous code, error codes "1↑↓", "0↑↓0", and "0↑↓↓" can be used to identify the nonlinear situations corresponding to them. It can be concluded that the input capacitance, C_{IN}, is out of range as soon as any one of these codes is detected.

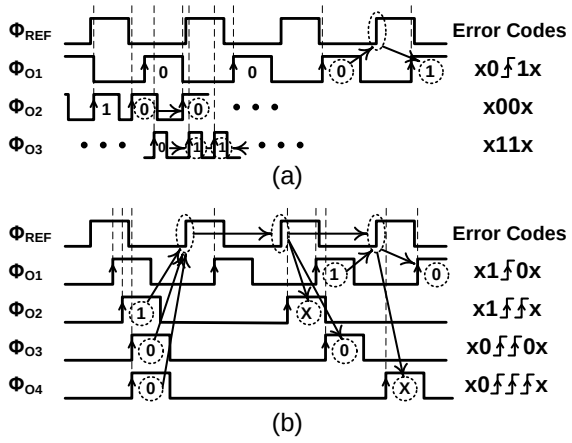
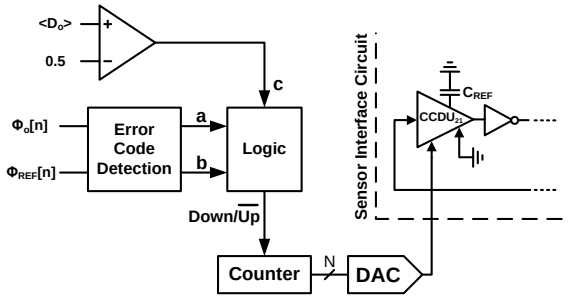


FIG. 11 (a) ERROR CODES TO DETECT A C_{IN}<$C_{IN,Min}$ SITUATION, (b) ERROR CODES TO DETECT A C_{IN}>$C_{IN,Max}$ SITUATION

The Algorithm to Tune for the Proper Equivalent Reference Capacitance Level

The initial capacitance reference level for different sensors might be different; also, the phase difference between the two ring oscillators can change due to transistor mismatches or aging over time. To avoid a trimming procedure after fabrication and to take full advantage of a cheap digital CMOS process, the control code developed in section III.B can be adopted to establish the appropriate equivalent reference capacitance level, $C_{REF,EQV}$, for an unknown sensor element and to enable process and mismatch errors to be compensated for.

As the output, <D_O>, ranges from 0 to 1 in some fractional value, it is appropriate to select the mid-range value of 0.5 to correspond to the desired reference level to maximize the dynamic range of circuit. On start-up, if the output is less than 0.5, $C_{REF,EQV}$ should be decreased by increasing the bias voltage of $CCDU_{21}$. On the other hand, if the output is greater than 0.5, $C_{REF,EQV}$ should be increased. During the comparison, the error codes described in section III.B are observed in real-time. If any one of the seven error codes of Fig. 11 is detected, the bias voltage for $CCDU_{21}$ is altered in the appropriate direction such that the output of the circuit is set to be 0.5. During normal sensing operation, the error codes are constantly monitored to see if the data remain valid.



a	b	c	Down/$\overline{Up}$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
~~1~~	~~1~~	~~0~~	**Undefined**
~~1~~	~~1~~	~~1~~	**Undefined**

(b)

FIG. 12 (a) THE CIRCUIT TO IMPLEMENT THE TUNING ALGORITHM. (b) THE TRUTH TABLE FOR THE LOGIC BLOCK IN PART (a)

In Fig. 12(a) a block diagram capturing the essence of the tuning algorithm is shown. The error code detection block checks the oscillator outputs to see if an error has occurred (see Fig. 11). If any of the errors listed in Fig. 11(a) or (b) occurs, the output bit flag *"a"* or *"b"* will be set to be *"1"*. These two flag bits and the output of the comparator *"c"* are forwarded to a logic block whose truth table is listed in Fig. 12(b). Due to the nature of the output error codes, the situation when both *a* and *b* are set to be *"1"* is undefined and should never happen. The output of the logic block is then used to set the proceeding counter to count up or down, depending on the action required, which directly alters the bias voltage of $CCDU_{21}$ through the DAC thereby establishing desired reference capacitance level.

Experimental Results

The final interface circuit, as illustrated in Fig. 13, is designed and implemented in 1-V, 90nm ST CMOS

technology. To satisfy Eqn. (28), identical bias voltages are used to bias $CCDU_{12}$, $CCDU_{22}$, $CCDU_{13}$, and $CCDU_{23}$. Voltage $V_{b\text{-}Sen}$ is used to control $CCDU_{11}$ in order to adjust the sensitivity of the circuit. $CCDU_{21}$ is controlled by $V_{b\text{-}Ref}$, the voltage responsible to establish the equivalent reference capacitance as explained earlier. To implement the control routines, Φ_O and Φ_{REF} are taken off of the chip through buffers. As explained earlier, these outputs will be used to detect error codes declaring the non-linear performance of the circuit.

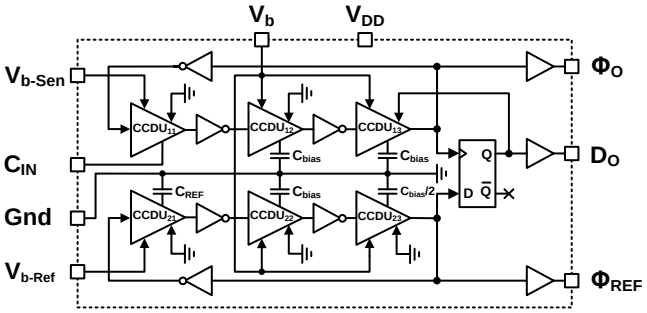


FIG. 13 THE COMPLETE DIAGRAM OF THE TIME-MODE DELTA-SIGMA INTERFACE

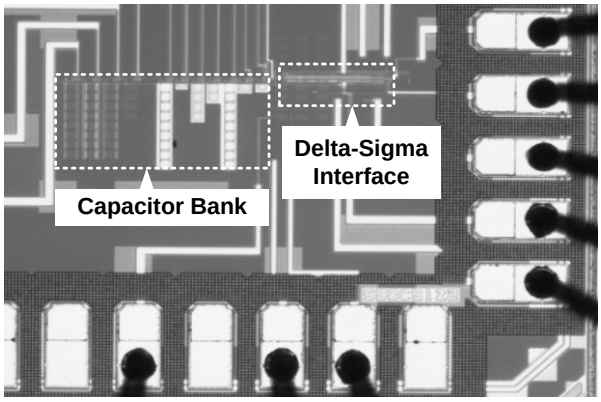


FIG. 14 THE MICROPHOTOGRAPH OF THE IMPLEMENTED DELTA-SIGMA INTERFACE

C_{REF} and C_{bias} capacitors have been implemented using 0.5 pF fringe-capacitors alongside a bank of capacitors on-chip consisting of 12.5 fF, 25 fF, 50 fF, 100 fF, 200 fF, 400 fF, 800 fF, 1 pF, 2 pF, 4 pF, and 7 pF fringe-capacitors. Depending on the test, a combination of these capacitors will be applied to the input pin C_{IN}. Generally, the test conditions consists of one input bias capacitor of values 0 pF, 1 pF, 2 pF, 4 pF or 7 pF together with some combination of the remaining capacitors called the signal capacitors. The signal capacitor components alter the input capacitance with respect to the input bias capacitance level (i.e. the signal with respect to a bias level). The sensor interface circuit should adapt $C_{REF,EQV}$ such that it equals the input bias capacitance level. A microphotograph of the die is shown in Fig. 14 and it occupies an area of 120 μm x 20 μm including the output buffers.

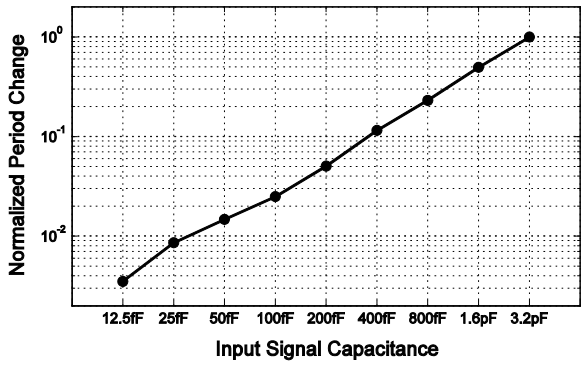


FIG. 15 THE CAPACITOR PROFILE OF THE IMPLEMENTED CAPACITOR BANK

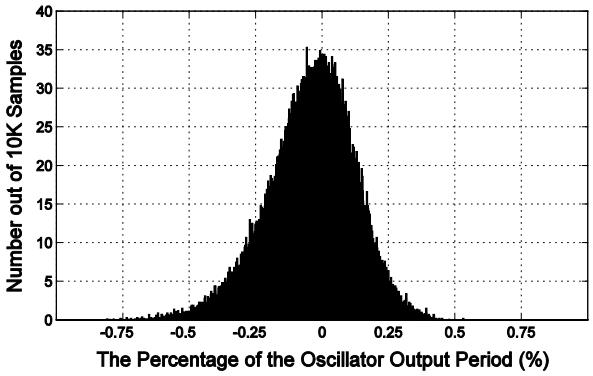


FIG. 16 THE JITTER NOISE ASSOCIATED WITH THE CIRCUIT

Each capacitor in the capacitor bank is individually characterized with respect to the open circuit situation whereby no capacitance is connected to the input pin C_{IN}. This was conducted by measuring the period of the signal oscillator. According to Eqns. (12)-(17), the expected change in the oscillation period is a linear function of the input capacitance C_{IN}. Using a *Le Croy* digital scope (model *SDA-6000*), the oscillation period for 10,000 cycles of Φ_O was measured and averaged to extract the actual capacitance value realized on-chip. For different bias voltages $V_{b\text{-}Sen}$ ranging from 0.3 to 0.7 V, the change in the oscillator period versus the input signal capacitance was determined and is shown in Fig. 15(a). Lines have been drawn between each data point for ease of illustration. Also, the x-axis represents the nominal capacitor values or bins drawn on a nonlinear axis for ease of reference. By dividing and normalizing each curve in Fig. 15(a) to its highest value, the plot in Fig. 15(b) was derived. As evident, all curves were normalized to essentially the same graph, indicating the linearity of the method used to characterize the various input capacitor values. This graph will be considered as the capacitor profile to be measured. Also in Fig. 16 and extracted out of 10,000 samples, the distribution percentage for the jitter associated with

each oscillating signal relative to the period of oscillation is shown. The distribution pattern is very much Gaussian with a zero mean and a standard deviation of 0.076% of the oscillation period.

To measure the integrated capacitor bank, this time the proposed sensor interface circuit was used. The test setup is shown in Fig. 17. The voltage at pin V_b is connected to a middle level voltage and the voltage at pins $V_{b\text{-}Sen}$ and $V_{b\text{-}Ref}$ are set using two different DACs. For any input capacitance, the output Φ_O and Φ_{REF} are forwarded to the control unit to make sure that the interface works in its linear mode. After assigning a voltage to $V_{b\text{-}Sen}$ through DAC_1 and using the tuning algorithm described earlier, the control unit modifies the input to DAC_2 to set the proper $C_{REF,EQV}$ such that it equals the input bias capacitance level. During this process, any mismatche between the two oscillators will be corrected, as well. The sensitivity of the sensor interface circuit is modified using DAC_1 such that the gain is maximized over some desired capacitance range. In our specific case, an external known signal capacitor is connected in parallel with some input bias capacitance and the sensor interface circuit output is monitored such that the slope of the output versus input signal capacitance reaches a desired level. Any modification in the sensitivity of the circuit should be followed by a tuning algorithm.

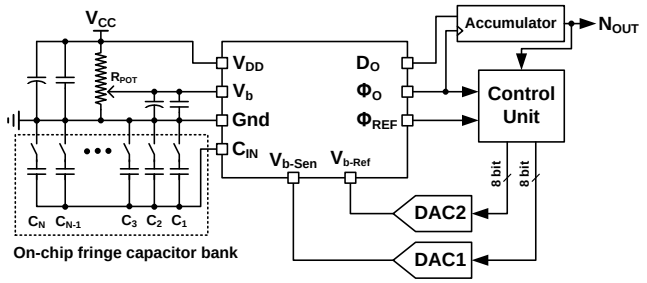


FIG. 17 THE DIAGRAM SCHEME FOR THE TEST CIRCUIT

The data captured by the sensor interface circuit is shown in Fig. 18(a) in normalized format. The input bias capacitance was varied within 0 pF, 1 pF, 2 pF, 4 pF and 7 pF while the input signal capacitance was varied from 0 pf to 800 fF. As evident, the data is very similar for each bias condition, again indicating very good linearity. The relative absolute error in percent was computed with respect to the curve derived earlier through the oscilloscope measurements associated with the oscillation period (Fig. 15(b)) and the results are shown in Fig. 18(b). Here the data is identified according to the input bias capacitance level. For small values of input signal capacitance, the relative error is greatest. It is also evident that the relative error is the largest when the input bias capacitance is at its maximum input value of 7 pF. These results appear to be consistent over several separate sets of measurements. This indicates that noise strongly affects the lower range of the measurements. This is not too surprising, as the variance of the jitter associated with each oscillator output is directly proportional to the input bias capacitance level as seen in Eqn. (37). This implies that the accuracy of the sensor interface is better at smaller input bias capacitance levels than that at larger ones.

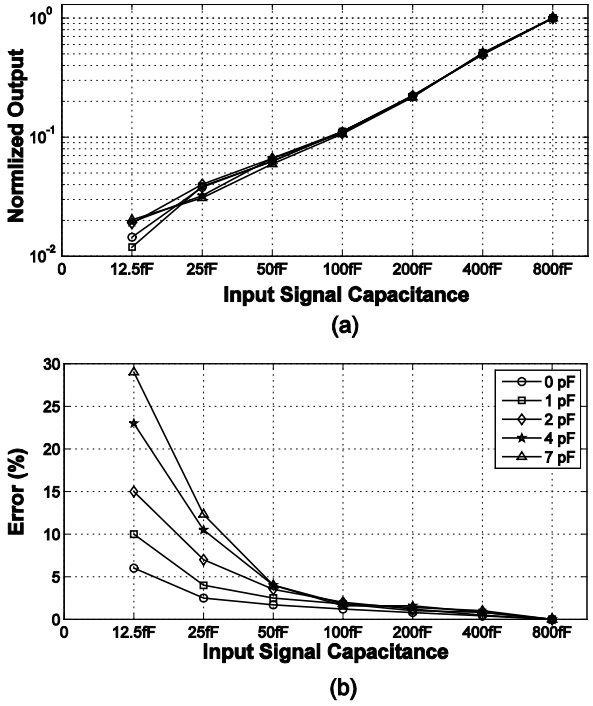


FIG. 18 (a) THE CHARACTERIZED INPUT C_{IN} BETWEEN ZERO AND 800 FF WITH DIFFERENT INPUT BIAS CAPACITANCE, (b) ABSOLUTE ERROR ASSOCIATED WITH MEASUREMENTS IN PART (a)

To illustrate the ability of the circuit to adjust its input range, the input to DAC_2 was changed to modify the sensitivity of the sensor interface circuit. Three specific examples are shown in Fig. 19 for $V_{b\text{-}Sen}$ equal to 0.32 V, 0.44 V and 0.51V. In all cases, the input bias capacitance was fixed to be 0 fF and the input signal capacitance was incrementally increased to a maximum value of 2 pF. Here it is evident how the upper bound on the input signal capacitance range was adjusted from 200 fF to 2 pF. When these three curves are compared, the capacitor profile extracted in Fig. 15(b), some error is evident. Specifically, at very small signal capacitance levels of 12.5 fF, the relative error varies from 2% to 67% as the sensitivity of the sensor interface circuit decreases (i.e., signal range increases).

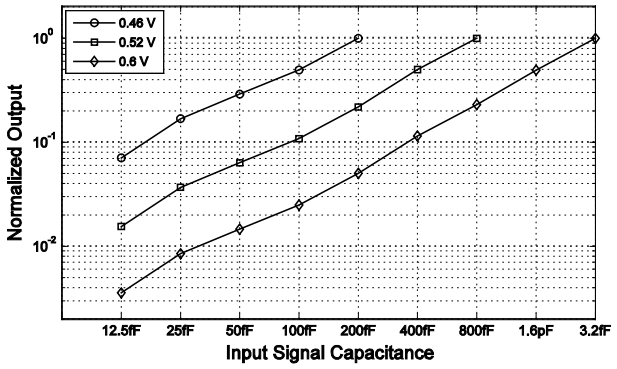


FIG. 19 DIFFERENT RANGES FOR INPUT CAPACITANCE MEASUREMENTS DUE TO DIFFERENT VALUES FOR $V_{b\text{-}Sen}$

Like any digital circuit, the static power consumption is a function of its operation frequency. By fixing the sampling frequency at 1 MHz, the power consumption was 110 μWatt. By scaling down the frequency to 300 kHz, the power consumption decreased to 34 μWatt. The fact that the operating frequency is externally tunable by adjusting the bias voltage V_b in Fig. 17 enables the power consumption of the sensor interface circuit to be adjustable as well. This, along with the very small silicon footprint, is an important contribution of this sensor interface circuit.

Conclusion

This paper explores the design and implementation of a generic semi-digital interface circuit for capacitive sensors in a 90 nm 1-V ST CMOS process. The design utilizes standard digital cells in association with capacitive-controlled delay units configured in a first-order sigma-delta loop. The design is synthesizable, portable across different technologies, reconfigurable on-the-fly and easy to calibrate. Moreover, the proposed circuit consumes as little as 34 μW operating a frequency of 300 kHz, and has a very small silicon footprint occupying 2400 μm^2. Finally, the circuit has been shown to be adjustable over power, sensitivity and input capacitance bias level, a feature unique to this work.

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Dr. Roberts has supervised over 50 graduate students at the Masters and PhD level. In 2003 he took leave from McGill to co-found DFT Microsystems, Inc, a company specializing in high-speed timing measurement. He returned to McGill 2005 where his current research includes analog IC design methods and built-in self-test techniques for analog and high-speed digital circuits. Dr. Roberts is a Fellow of the IEEE.